CLAIMS

What is claimed is:

1. A method for forming a die, the method comprising:

forming a die on a wafer, said die having an active portion comprising integrated circuitry, wherein said die has at least one input bond pad formed on said active portion;

forming at least one test pad on said die;

forming a conductive path between said at least one input bond pad and said at least one test pad, wherein a portion of said conductive path is formed on said die outside of said active portion of said die.

2. The method of claim 1, said forming at least one test pad comprises forming at least one test pad on said active portion of said die.

3. The method of claim 2, said active portion being surrounded by an inactive portion, wherein said conductive path extends from said at least one input bond pad to said inactive portion and from said inactive portion to said at least one test pad.

4. The method of claim 1, wherein said portion of said conductive path is formed on said wafer outside of said die.

5. The method of claim 1, further comprising severing said conductive path at a point outside of said active portion of said die.

6. The method of claim 3, further comprising severing said conductive path at a point within said inactive portion.

7. The method of claim 4, further comprising severing said conductive path at a point outside said die.

8. The method of claim 1, wherein said at least one test pad is of a sufficient size so as to be accessible by a testing apparatus.

9. A die assembly formed on a wafer, the die assembly comprising:

a die formed on the wafer, said die having an active portion comprising integrated circuitry;

at least one input bond pad formed on said active portion of said die;

at least one test pad formed on said die;

a conductive path that electrically couples said at least one input bond pad to said at least one test pad, wherein a portion of said conductive path is formed outside of said active portion of said die.

10. The die assembly of claim 9, wherein said at least one test pad is formed on said active portion of said die.

11. The die assembly of claim 10, said active portion of said die being surrounded by an inactive portion of said die, wherein said conductive path extends from said at least one input bond pad to said inactive portion and from said inactive portion to said at least one test pad.

12. The die assembly of claim 9, said die being surrounded by a non-conducting scribe area of the wafer, wherein said portion of said conductive path is formed on said non-conducting scribe area.

13. The die assembly of claim 9, wherein said at least one test pad is of sufficient size so as to be accessible by a testing apparatus.

14. A method for preparing a die on a wafer for testing by a testing apparatus, the method comprising:

forming a die on a wafer, said die having an active portion comprising integrated circuitry;

forming a plurality of input bond pads on said active portion;

forming a plurality of test pads on said die, said plurality of test pads accessible to the testing apparatus, at least one of said plurality of test pads corresponding to at least one of said plurality of input bond pads;

forming a conductive path between said at least one of said plurality of test pads and said at least one of said plurality of input bond pads, wherein a portion of said conductive path is formed outside of said active portion of said die; and

testing said die by contacting said at least one of said plurality of test pads with the testing apparatus.

15. The method of claim 14, wherein said plurality of test pads is formed on said active portion of said die.

16. The method of claim 14, said active portion being surrounded by an inactive portion, wherein said portion of said conductive path is formed on said inactive portion.

17. The method of claim 14, wherein said portion of said conductive path is formed on said wafer outside of said die.

18. The method of claim 14, further comprising severing said conductive path at a point outside of said active portion of said die.

19. The method of claim 16, further comprising severing said conductive path at a point within said inactive portion.

20. The method of claim 17, further comprising severing said conductive path at a point outside said die.

21. The method of claim 14, wherein said at least one of said plurality of test pads is larger in size than said at least one of the plurality of input bond pads.

22. A die comprising:

an active portion comprising integrated circuitry;

a plurality of input bond pads formed on said active portion;

a plurality of test pads formed on said die;

a plurality of conductive lines, wherein each of said conductive lines is initially formed to electrically couple at least one of said plurality of input bond pads to at least one of said plurality of test pads, and wherein a portion of said each of said conductive lines is formed on an area outside said active portion of the die and is subsequently severed at a point outside said active portion of the die.

23. The die of claim 22, said plurality of test pads formed on said active portion of said die.

24. The die of claim 22, said active portion being surrounded by an inactive portion, wherein said portion of each of said conductive lines is formed on said inactive portion and is subsequently severed at a point on said inactive portion.

25. The die of claim 22, wherein said portion of said each of said conductive lines is formed outside of the die and is subsequently severed at a point outside the die.

26. The die of claim 25, the die being formed on a wafer, wherein said portion of said each of said conductive lines is severed when the die is separated from said wafer.

27. The method of claim 22, wherein said at least one of said plurality of test pads is larger in size than said at least one of said plurality of input bond pads.